

Fig. 3A

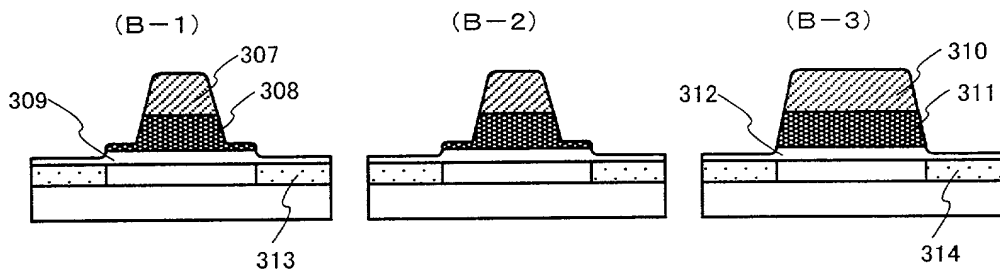


Fig. 3B

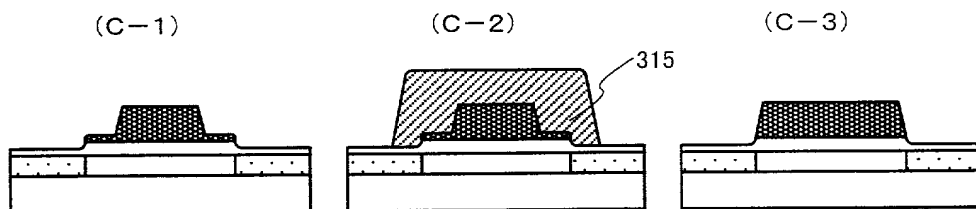


Fig. 3C

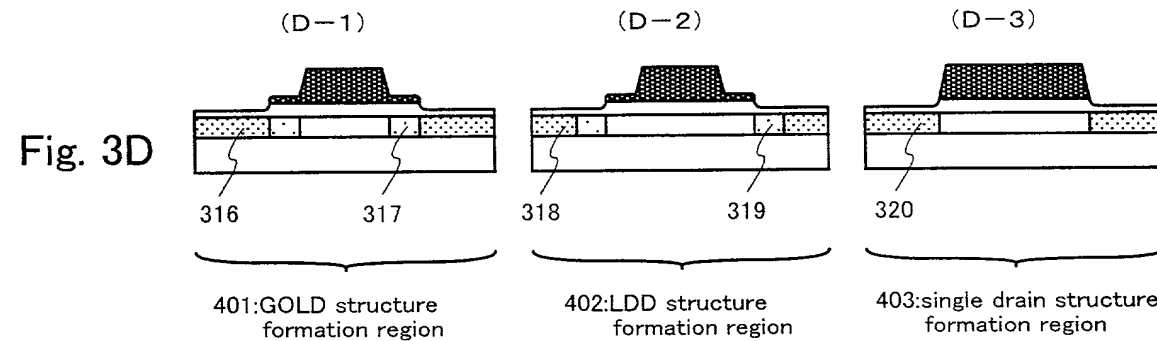


Fig. 3D

506 : shift register circuit (GOLD structure)  
507 : level shifter circuit (GOLD structure)  
508 : buffer circuit (GOLD structure)

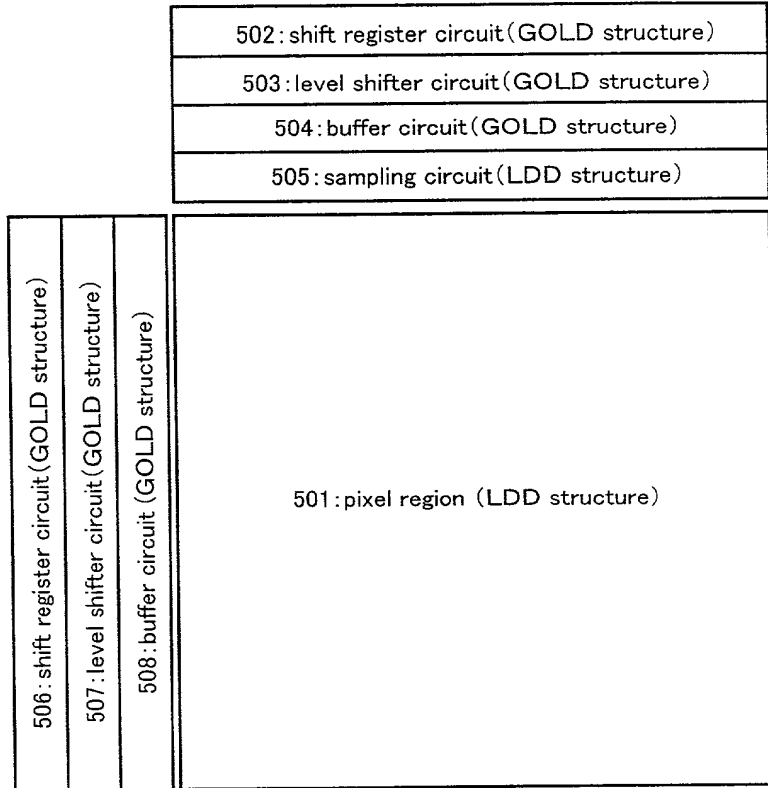


Fig. 4

Fig. 5A

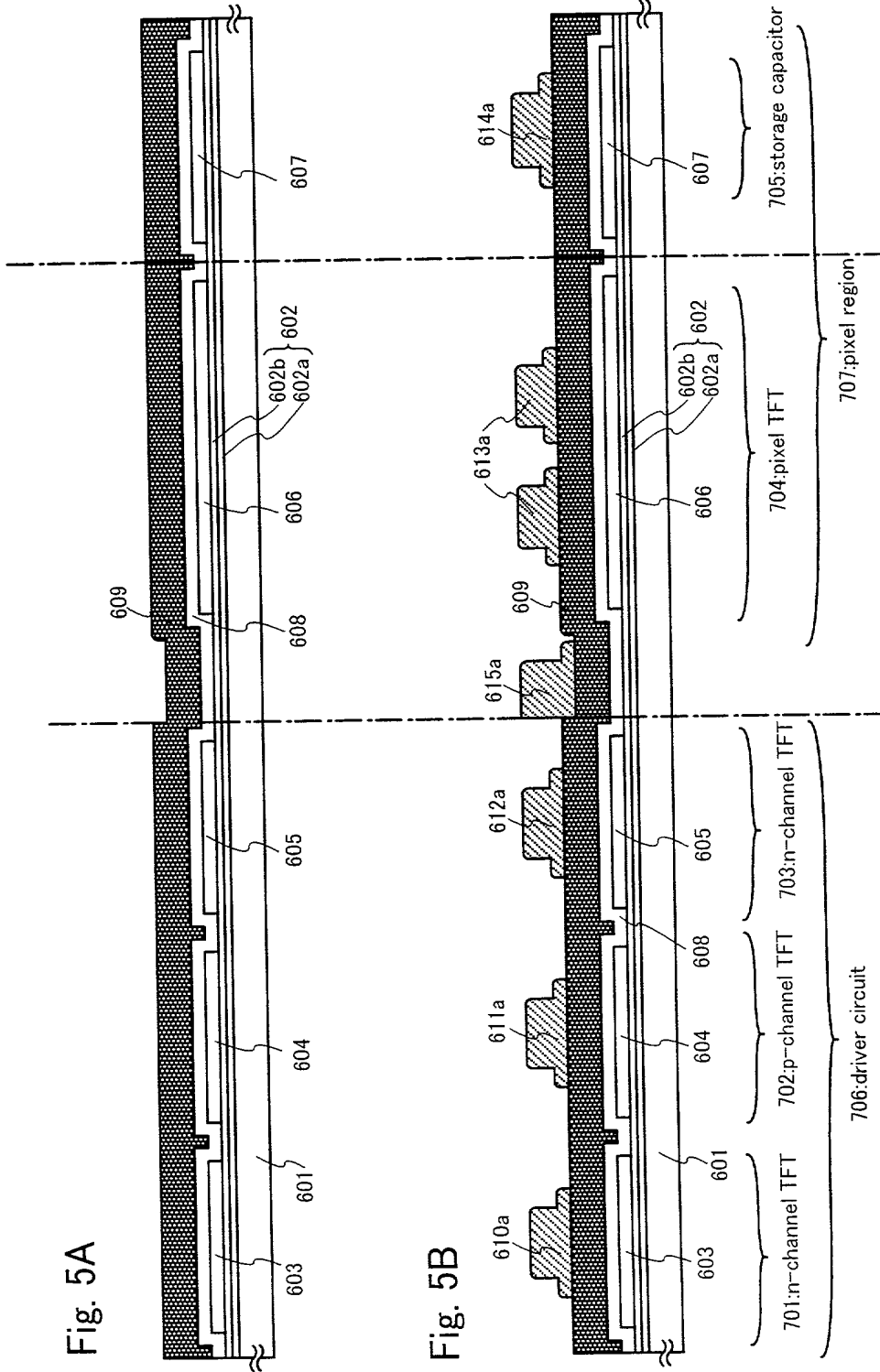


Fig. 5B

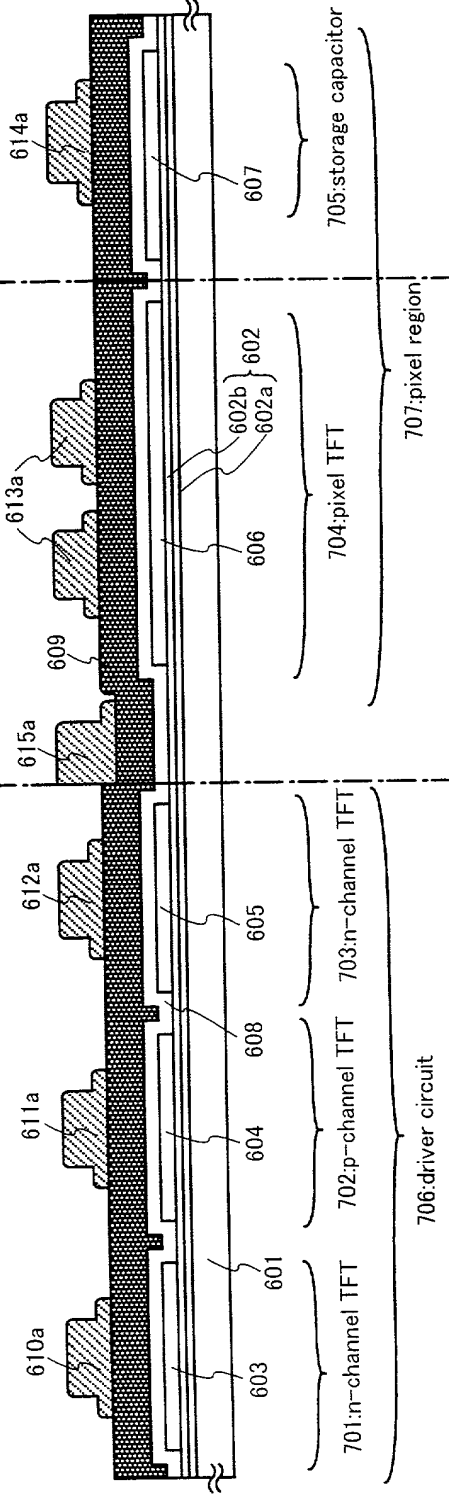




Fig. 7A

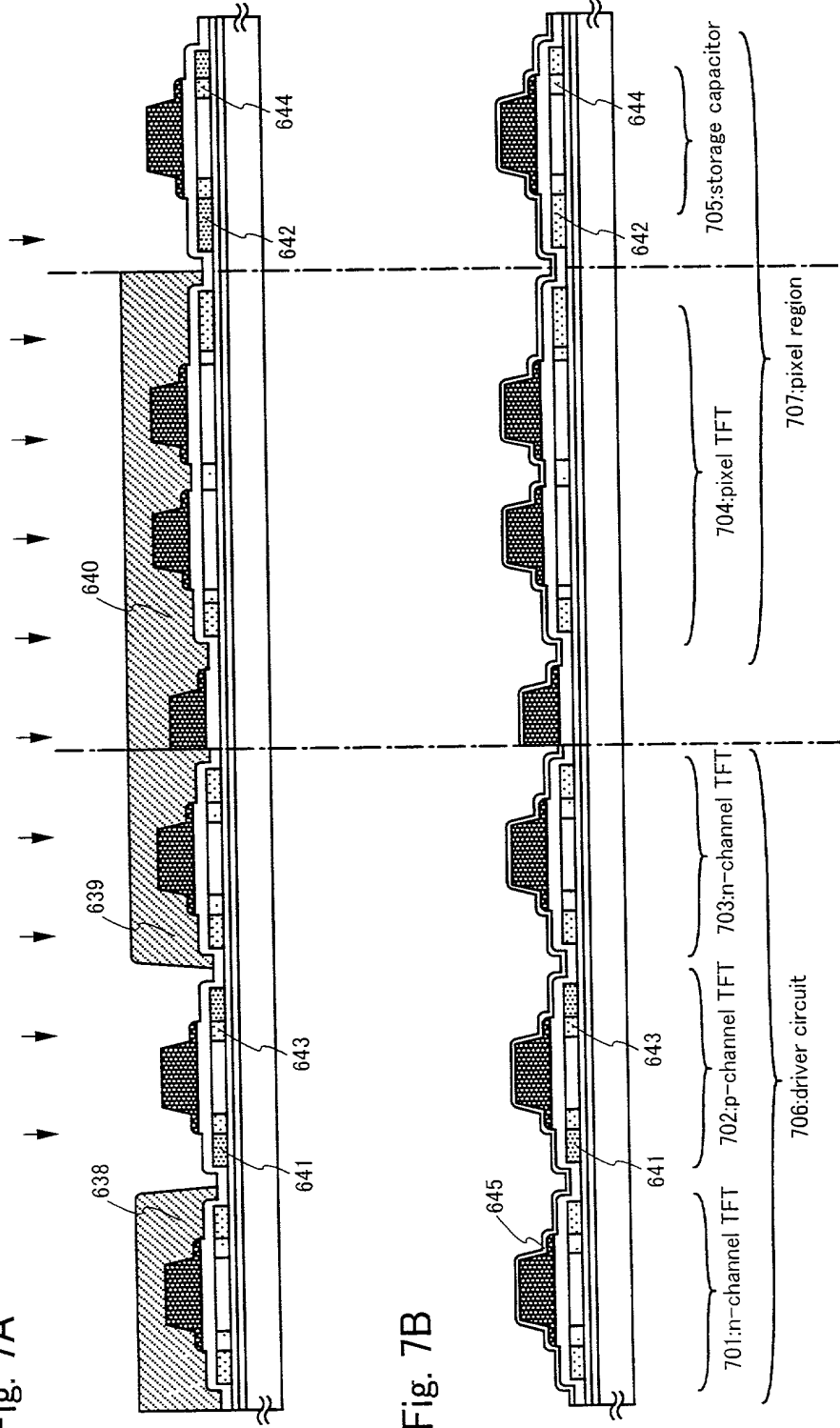


Fig. 7B

Fig. 8A

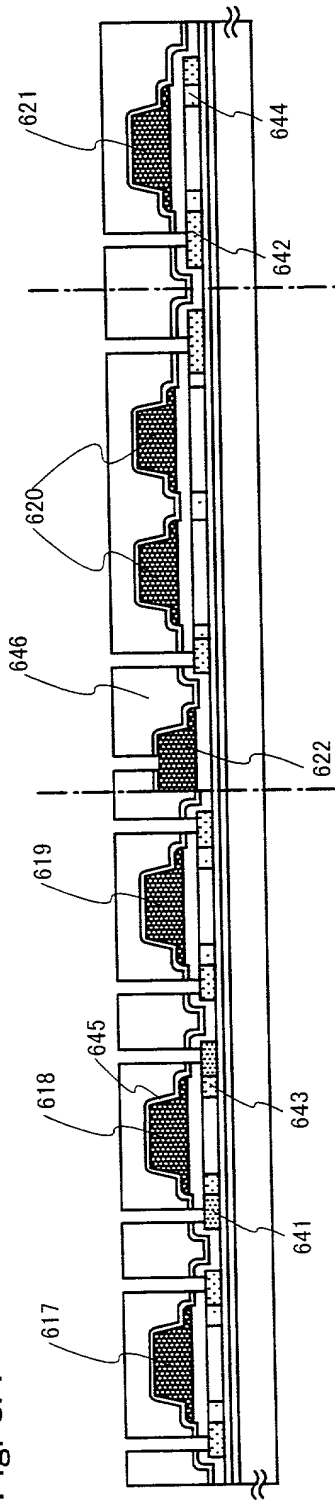


Fig. 8B

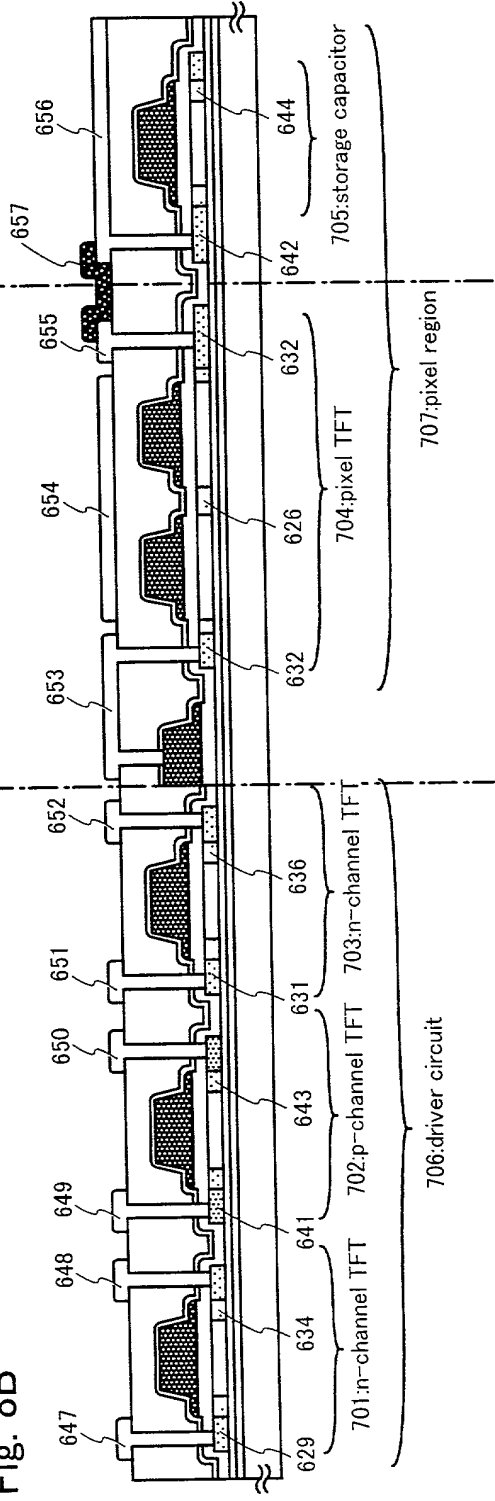




FIG. 9A  
FIG. 9B  
FIG. 9C  
FIG. 9D  
FIG. 9E

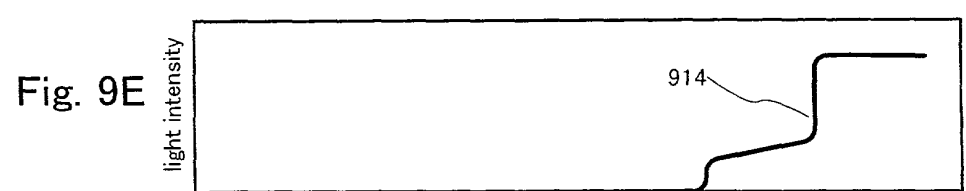
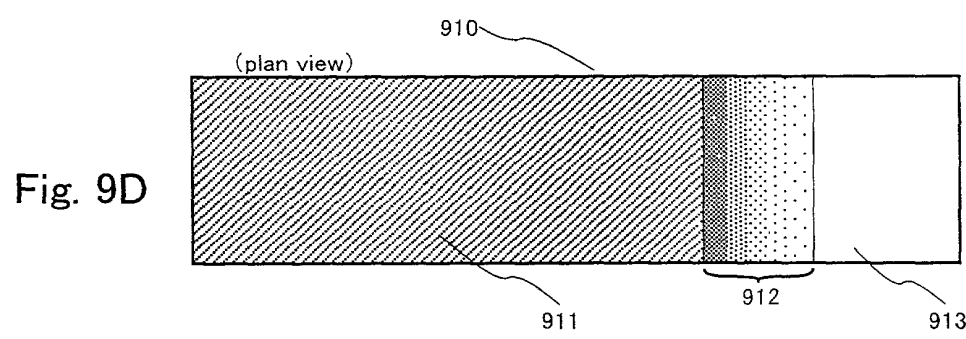
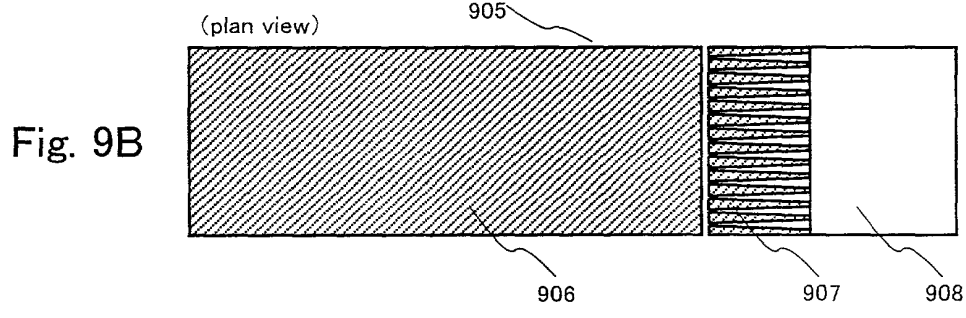
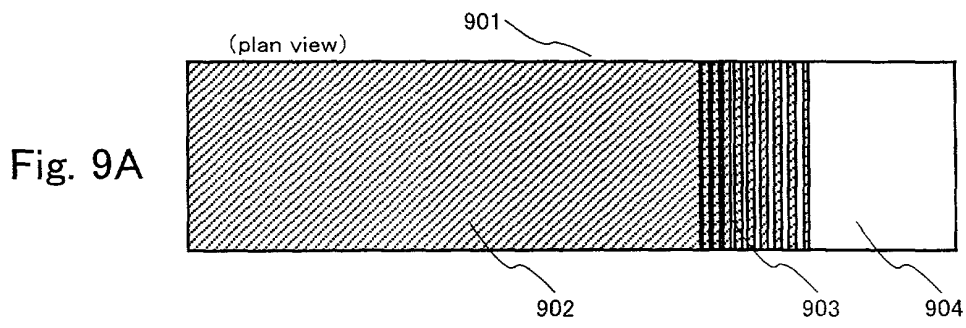


Fig. 10A

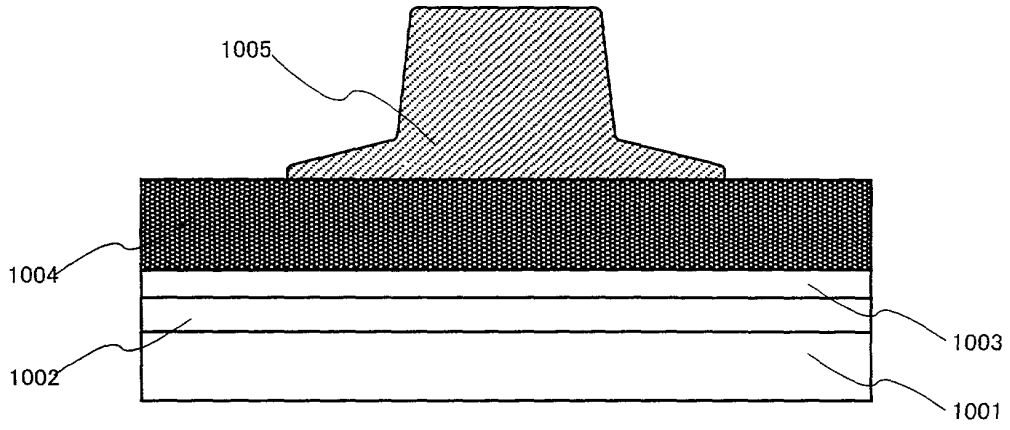


Fig. 10B

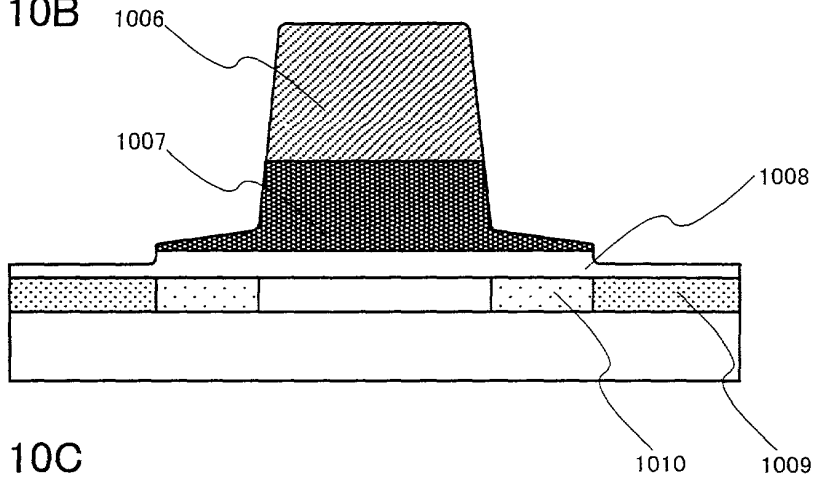


Fig. 10C

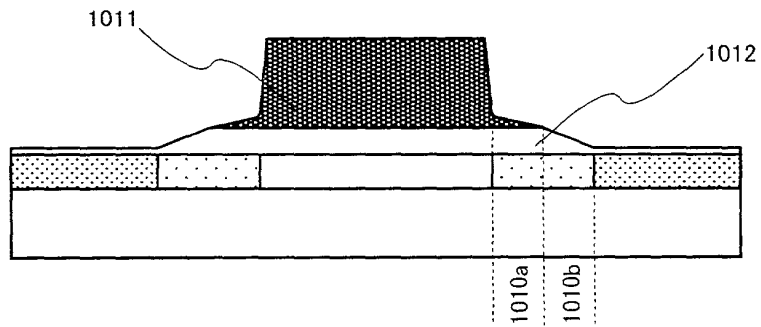


FIG. 11A

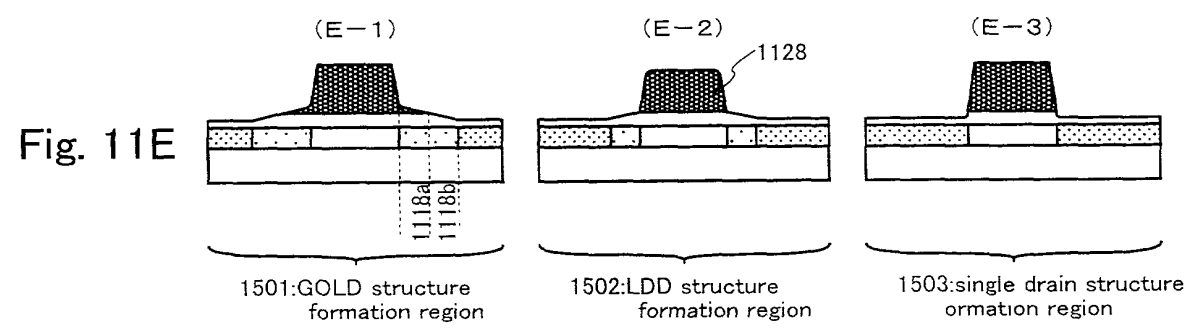
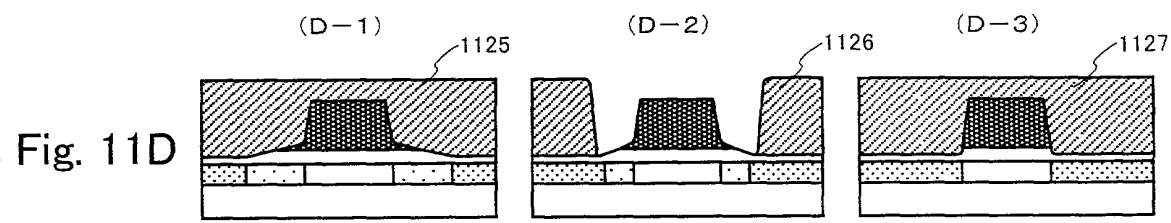
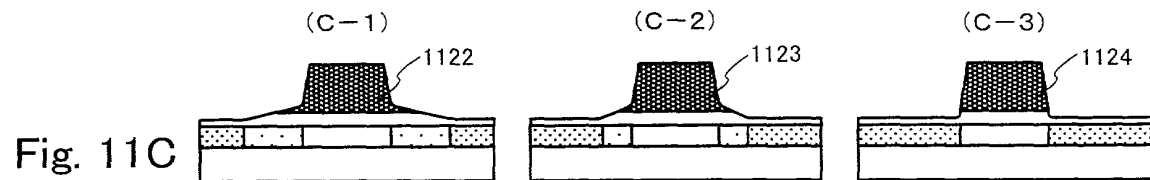
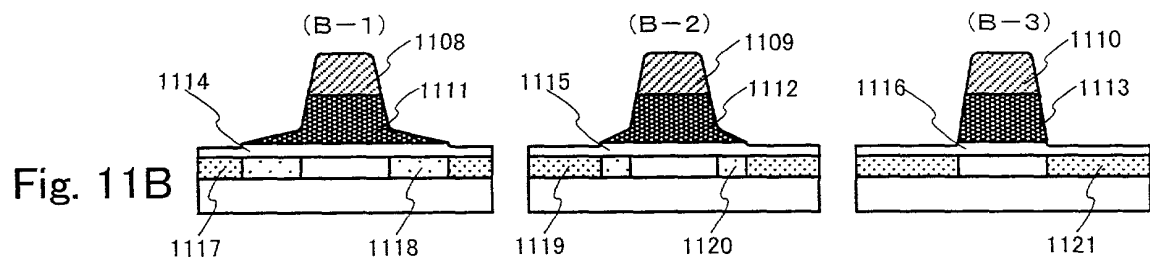
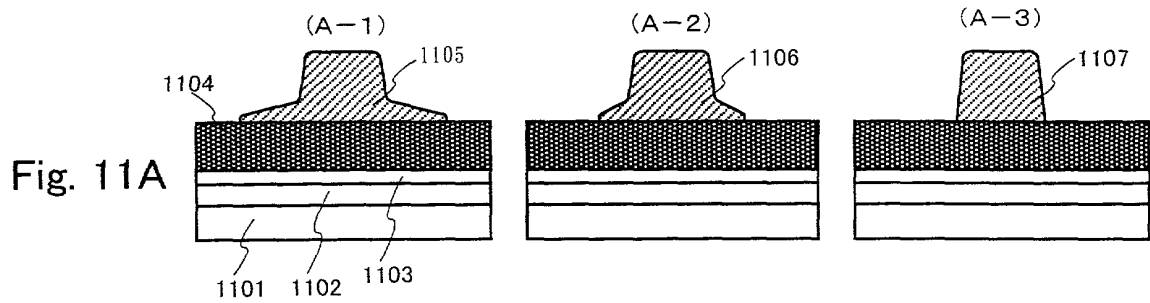


Fig. 12A

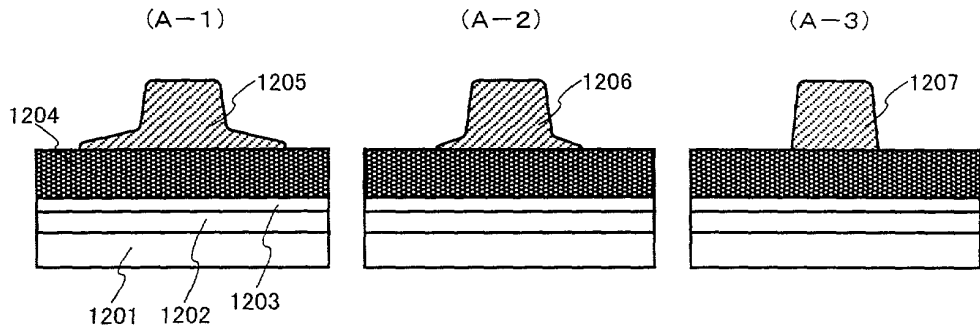


Fig. 12B

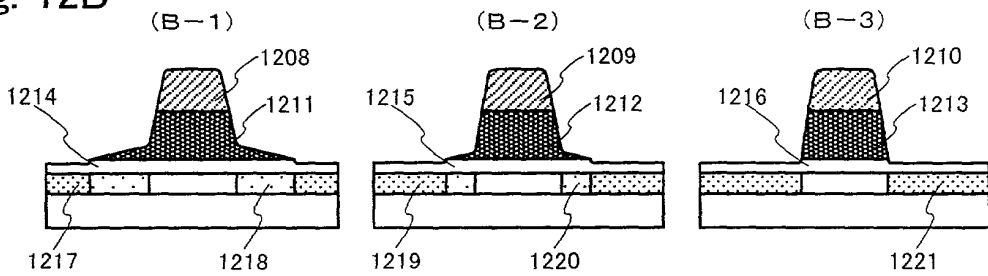
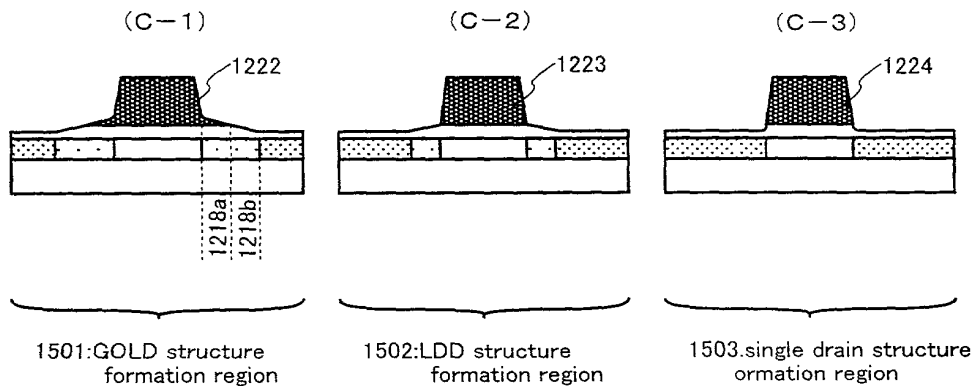


Fig. 12C



"Patent" of "Patent"

Fig. 13A

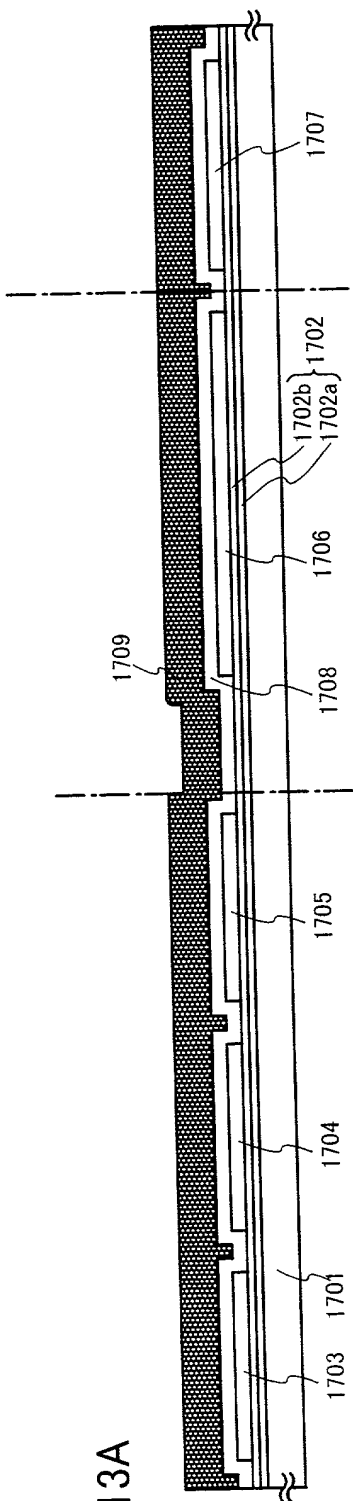
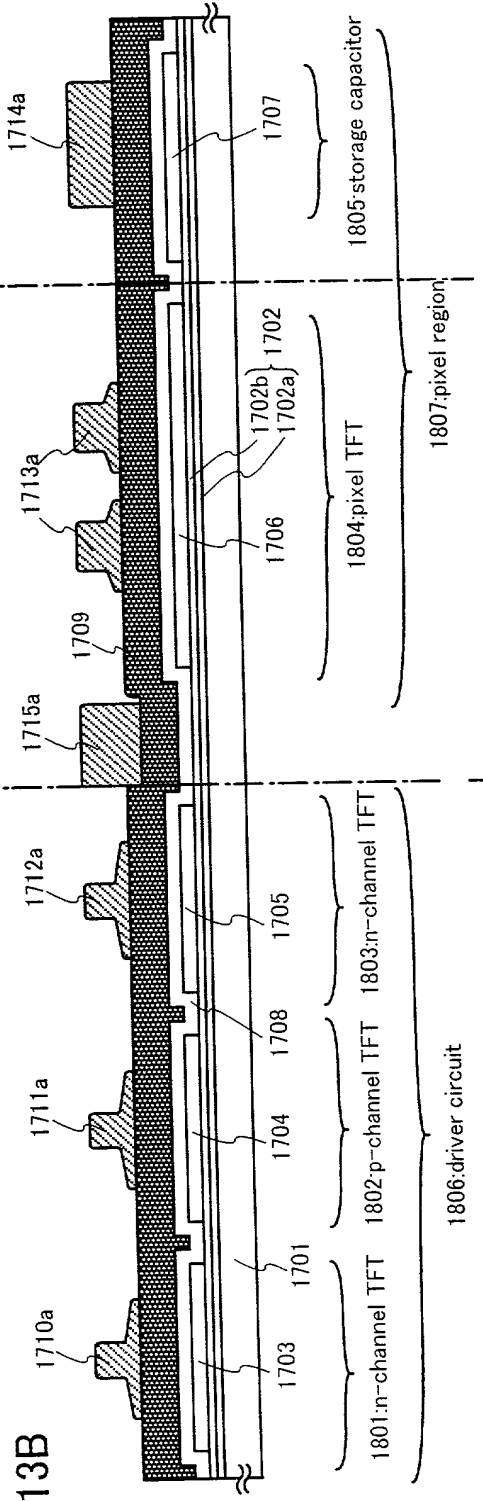


Fig. 13B



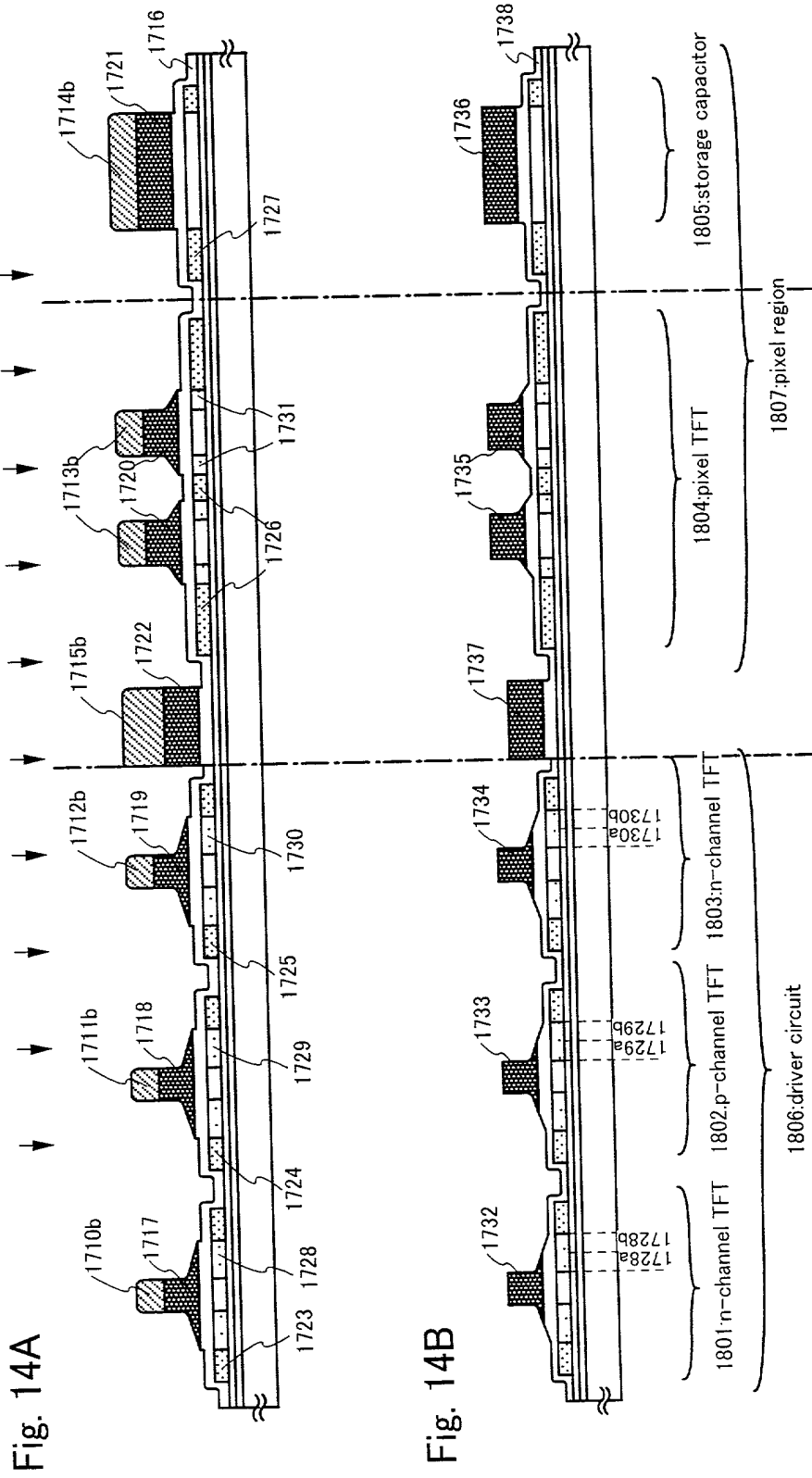


Fig. 14A

Fig. 14B

Fig. 15A

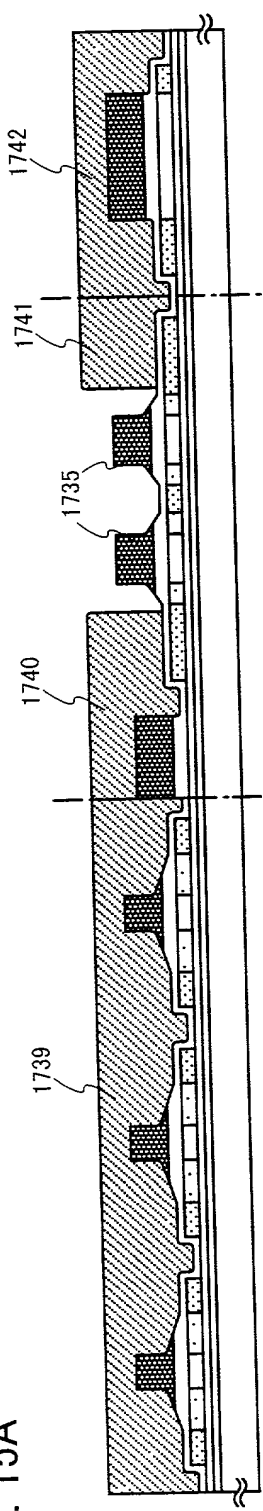


Fig. 15B

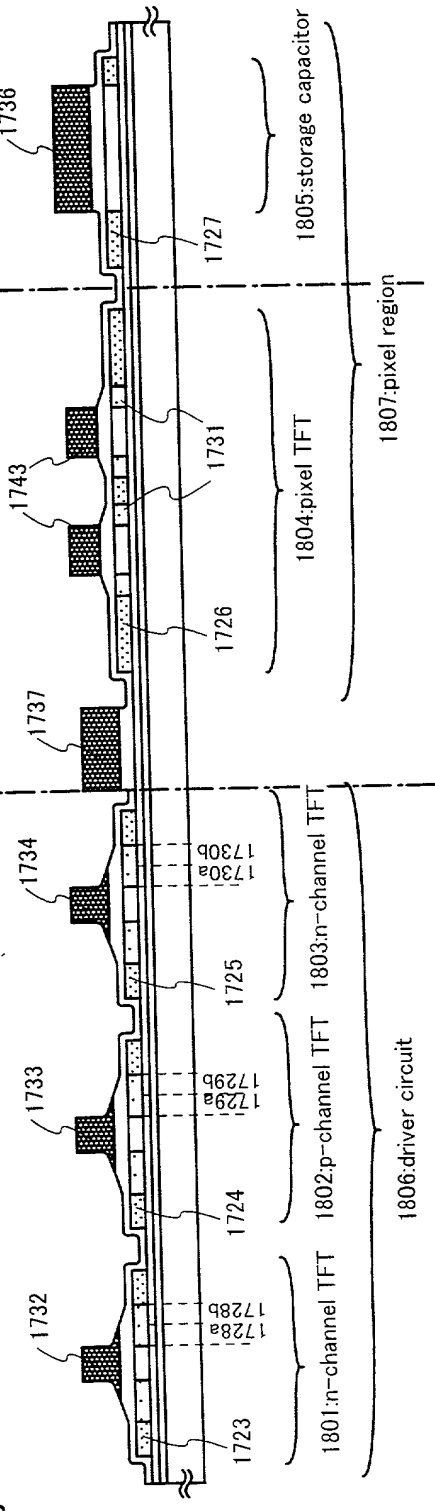


Fig. 16A

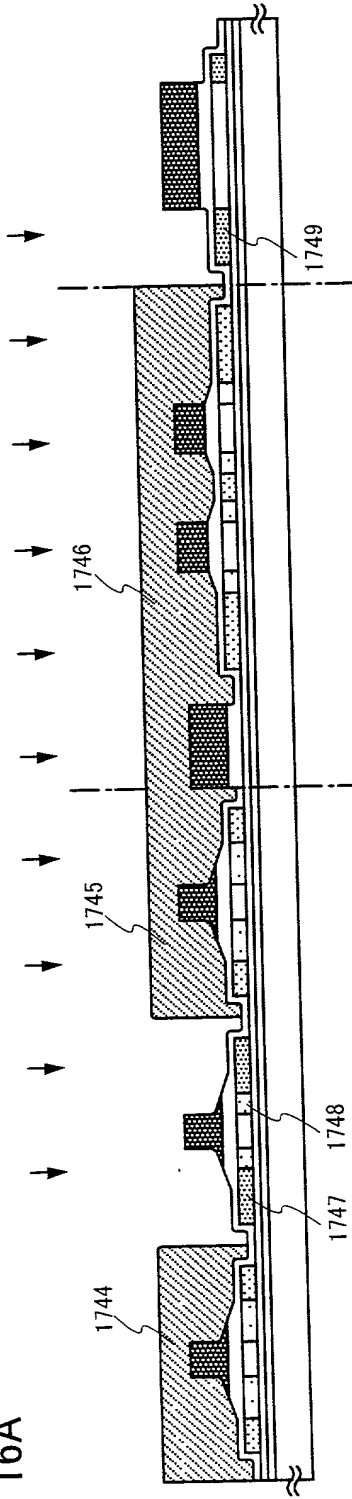
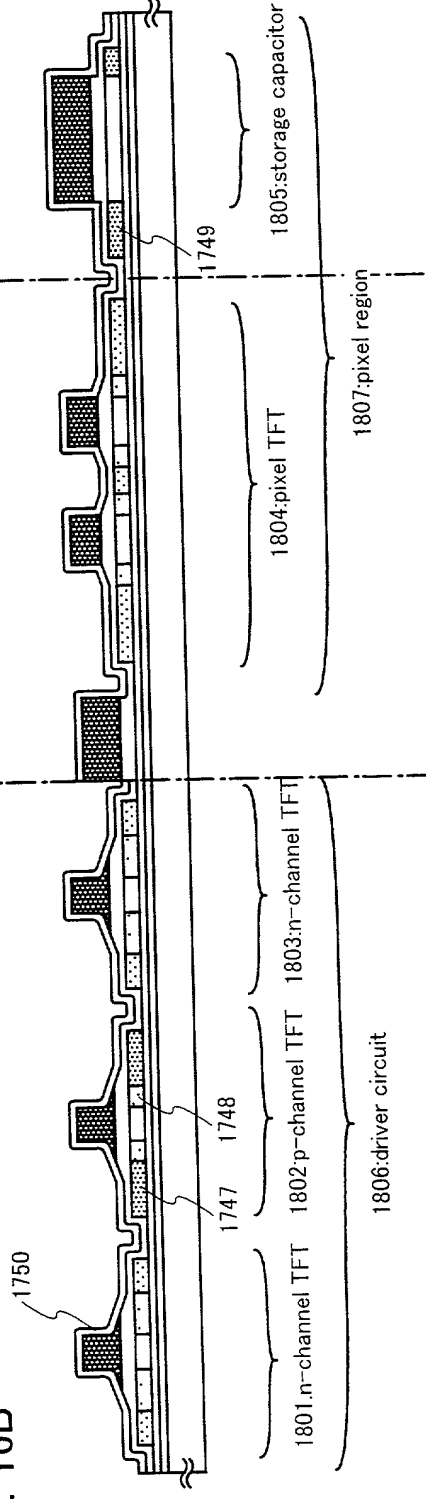


Fig. 16B



1801:n-channel TFT 1802:p-channel TFT 1803:n-channel TFT 1804:pixel TFT  
1805:storage capacitor  
1806:driver circuit  
1807:pixel region





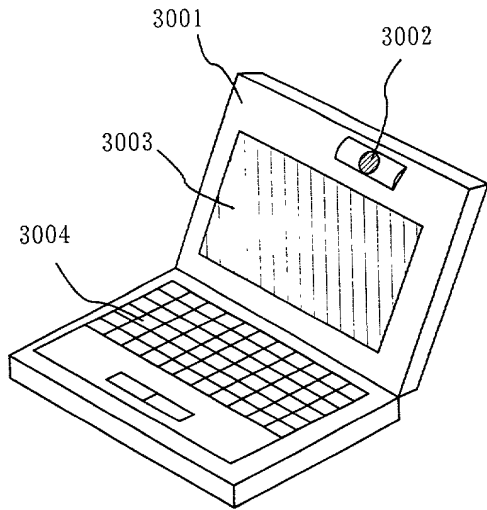


Fig. 18A

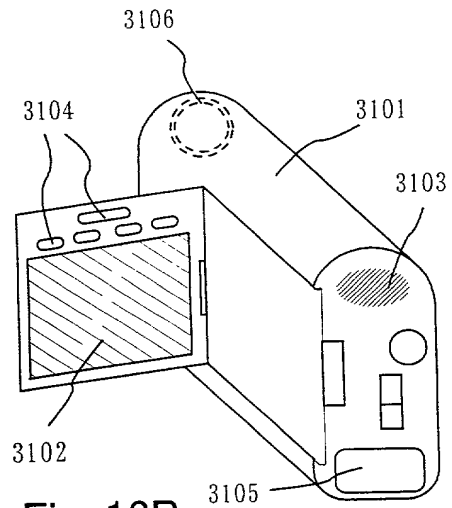


Fig. 18B

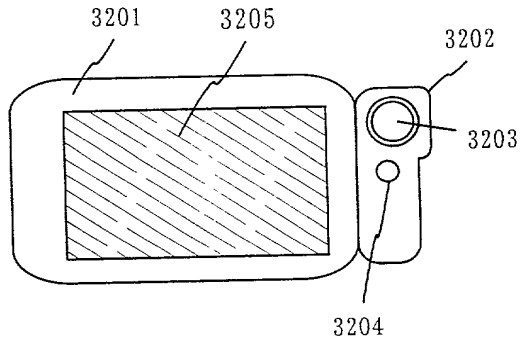


Fig. 18C

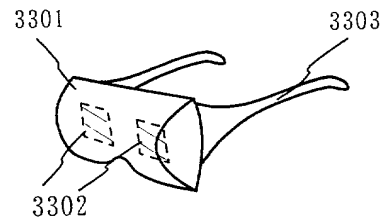


Fig. 18D

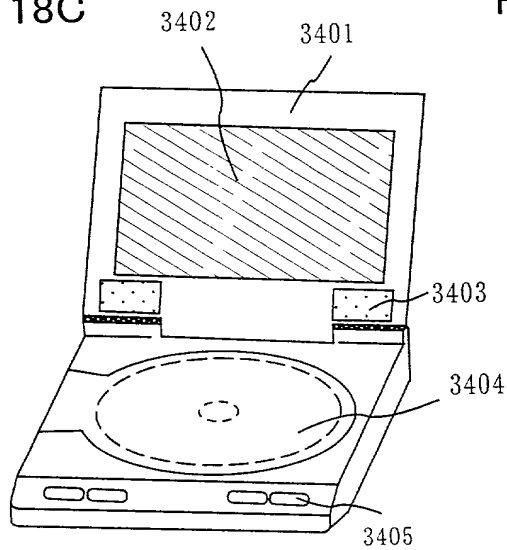


Fig. 18E

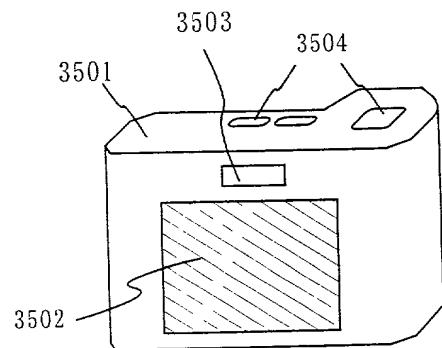


Fig. 18F

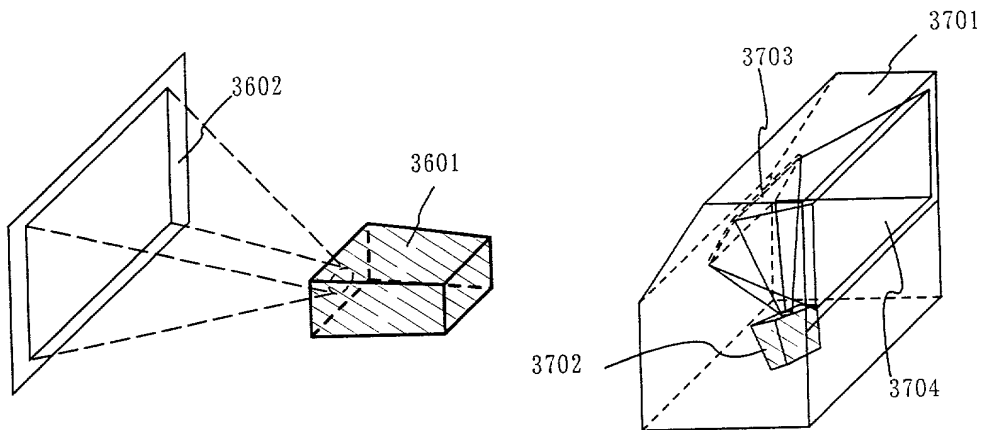


Fig. 19A

Fig. 19B

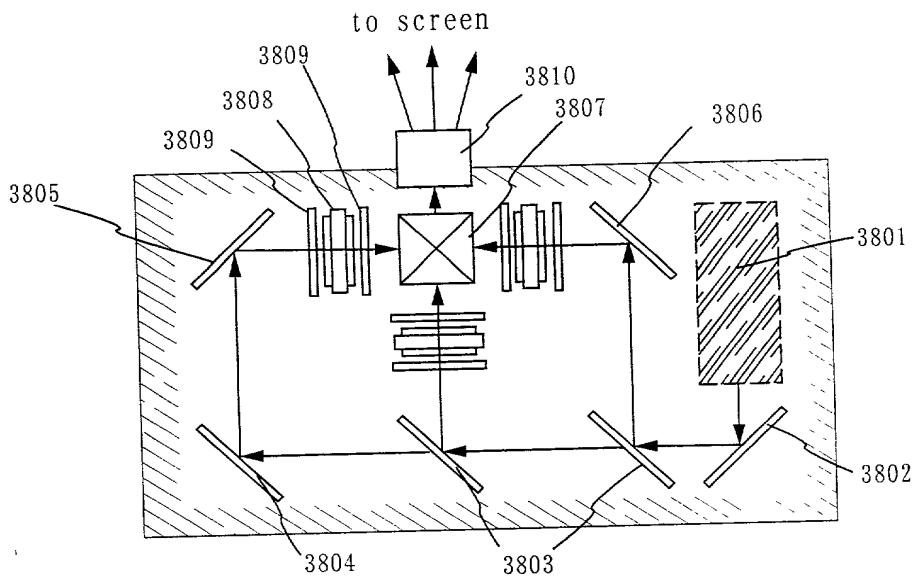


Fig. 19C

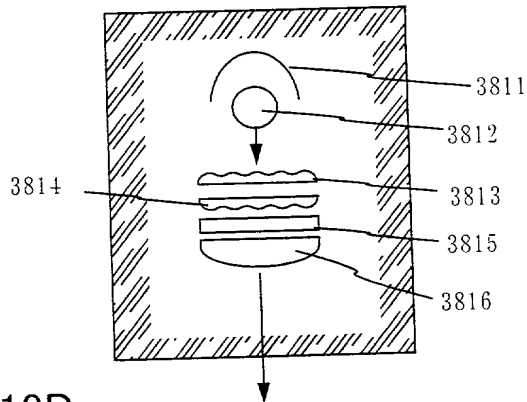


Fig. 19D

Fig. 20A

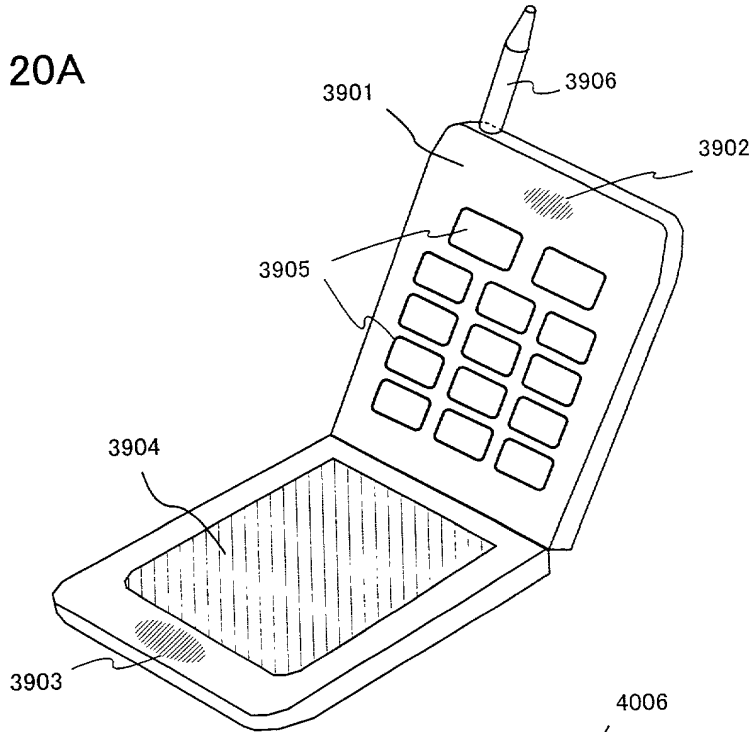


Fig. 20B

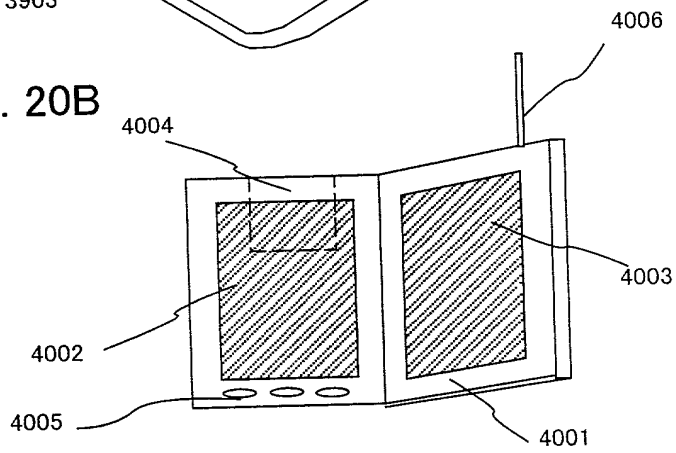


Fig. 20C

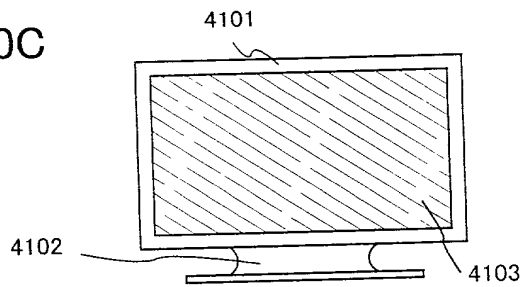


Fig. 21A

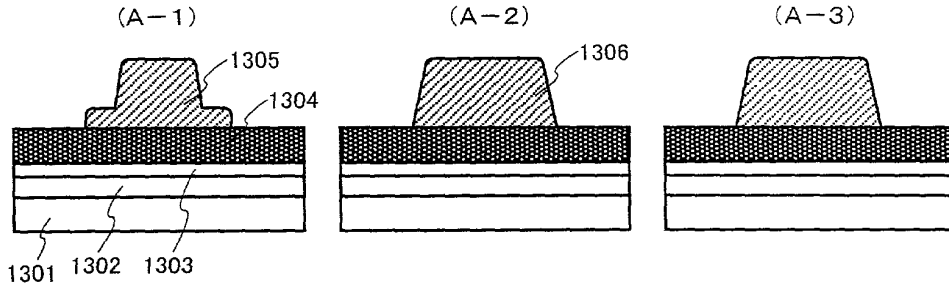


Fig. 21B

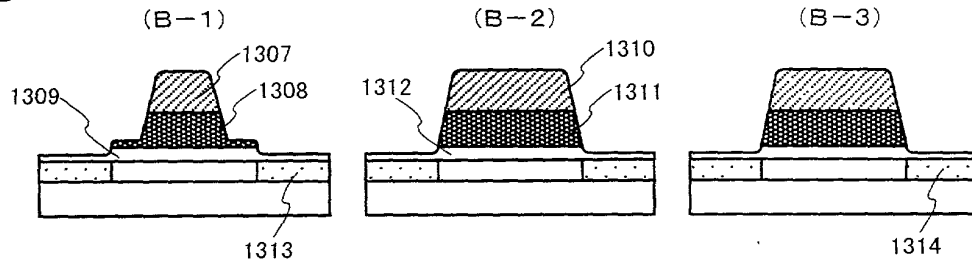


Fig. 21C

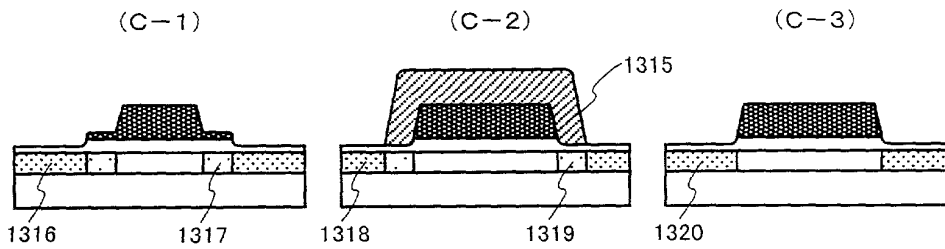


Fig. 21D

